CLAIMS

1. An apparatus comprising:

a clock generation circuit configured to generate an output clock signal in response to a control signal;

a detect circuit configured to generate a detect signal in response to (i) said output clock signal and (ii) an input signal; and

a select circuit configured to generate said control signal by selecting (i) a first input when in a first mode (ii) said detect signal when in a second mode, wherein said first and second mode are selected in response to a selection signal.

2. The apparatus according to claim 1, wherein said select circuit further responds to a second input when either said first input or said detect signal are not present.

3. The apparatus according to claim 1, wherein said first mode comprises a read mode and said second mode comprises a wobble mode.

4. The apparatus according to claim 1, wherein said clock generation circuit comprises an analog clock generation circuit.

5. The apparatus according to claim 1, wherein said clock generation circuit comprises (i) a loop filter and (ii) a voltage controlled oscillator (VCO).

6. The apparatus according to claim 1, wherein said clock generation circuit is configured to generate said output signal when in said first mode, said second mode and said third mode.

7. The apparatus according to claim 1, wherein said clock generator circuit comprises:

a first loop filter;

a second loop filter; and

a voltage controlled oscillator.

8. The apparatus according to claim 1, wherein said clock generator circuit comprises:

a digitally controlled oscillator.

9. The apparatus according to claim 1, further comprising:

a phase circuit configured to generate a phase error signal in response to said output signal and a second control signal.

10. An apparatus comprising:

a clock generation circuit configured to generate an output clock signal in response to a first control signal; and

a phase circuit configured to generate a phase error signal in response to said output signal and a second control signal.

11. The apparatus according to claim 9, wherein said first control signal comprises a read channel signal and said second control signal comprises a wobble signal.

12. The apparatus according to claim 10, further comprising:

a variable delay circuit configured to delay said output clock signal in response to said phase error signal.

13. The apparatus according to claim 10, wherein said phase circuit comprises:

a phase select circuit;

a first and second integration circuit, each configured to present phase signals; and

a computation circuit configured to generate a phase calculation signal in response to said phase signals.

14. The apparatus according to claim 13, wherein said phase select circuit generates said phase error signal in response to said phase calculation signal.

15. A method for synchronizing a signal, comprising the steps of:

(A) generating an output clock signal in response to a control signal;

(B) generating a detect signal in response to (i) said output clock signal and (ii) an input signal; and

(C) generating said control signal by selecting (i) a first input when in a first mode (ii) said detect signal when in a third mode, in response to a selection signal.